

Front-End per rivelatori a semiconduttore

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Introduzione:

L'elettronica di lettura per rivelatori a stato solido con grande "granularita" ha avuto origine negli anni 70 in esperimenti di fisica delle alte energie.

Per esempio i quark **CHARM e BEAUTY** formano con altri quark **mesoni e barioni instabili** che poi decadono con vite medie di ~ 1 psec.

- → rivelatori "veloci" che sappiano misurare il passaggio di particelle relativistiche a minima ionizzazione con la precisione di alcuni micron
- → vita media del picosecondo per queste particelle "pesanti" significa spostamenti di qualche millimetro dal punto di produzione al punto di decadimento (transverse decay lenght)
- \rightarrow grande numero di elementi sensibili su un unico rivelatore + vari strati di rivelatori per avere alta risoluzione spaziale (aree sensibili ~ $0.1 0.2 \text{ m}^2$)
- → molti canali di lettura (circuiti "ibridi" a film spesso)

Tutti i moderni esperimenti usano rivelatori a stato solido

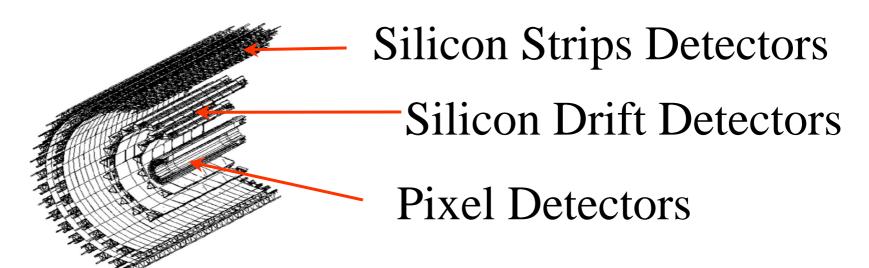
- → come rivelatori di vertice e "tracker" (aree sensibili >> 1 m², circuiti di lettura a VLSI)
- → materiale "tipico" e' ancora il Silicio (alta resistivita'), ma altri materiali sono di interesse (GaAs, CdZnTe, HgI2, CVD diamond, ...)



Rivelatori di vertice (e di traccia):

I tipi di rivelatori piu' comunemente usati sono:

- Rivelatori a "strisce" (singola e doppia faccia)
- Rivelatori a "pixel"
- Rivelatori a "pad" (large pixel ~ 1 mm x 1mm)
- Camere a deriva in Silicio
- CCD (Charge Coupled Devices)
- → Generalmente il rivelatore di vertice e' costituito da piu' di un tipo di rivelatore.
- → Ogni tipo di rivelatore e' a sua volta costituito da 3-4 strati di rivelazione





Caratteristiche importanti:

Le caratteristiche dei rivelatori dipendono un po' dall'applicazione:

→ La risoluzione spaziale e' chiaramente il parametro piu' importante per i rivelatori di vertice

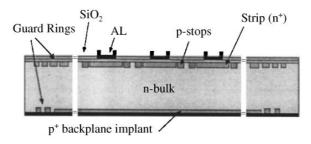
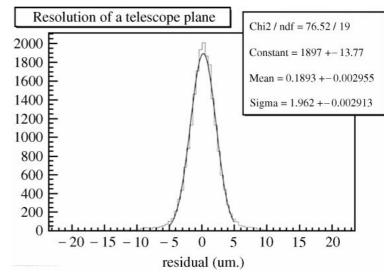


Fig. 10. Layout of a strip detector with strips on n⁺-side with p-stop ohmic separation.

Una delle migliori risoluzioni ottenute con un rivelatore a microstrip e':

$$\sigma = 1.4 \ \mu m$$
 Spessore
$$300 \ \mu m$$
 Pitch
$$25 \ \mu m$$
 Readout Pitch
$$50 \ \mu m$$
 Peaking time
$$\sim \mu s$$





Caratteristiche importanti per i rivelatori di traccia:

→ Per una ricostruzione efficiente e precisa del "b-tagging" e del "b-trigger", il parametro importante e' la risoluzione sullo "impact parameter d"

(la distanza trasversa retroproiettata fra il vertice primario ed il vertice di decadimento)

Es. 1. DELPHI, double-sided strip detectors

$$\sigma_{\rm d}(r\phi) = 21 \,\mu{\rm m}$$

$$\sigma_{\rm d}(z) = 36 \,\mu{\rm m}$$

per un decadimento a 90° di $Z^{\circ} \rightarrow \mu + \mu -$

2. ATLAS, pixel detector

$$\sigma_{\rm d}(r\phi) = 11 \,\mu{\rm m}$$

3. B-factory asimmetriche

$$\sigma_{\rm d}(z)$$
 < 130 μm

fra due vertici di mesoni B (separazione longitudinale)

→ Per rivelatori ad LHC cio' che conta e' soprattutto una buona efficienza nella ricostruzione delle tracce, buon pattern recognition e bassa occupanza

Es. CMS

$$\sigma = 15-25$$
 μm per ottenere una risoluzione sul momento trasverso di δp,/p, ~ 15 p, (TeV)%

→ Una nuova richiesta per i rivelatori di vertice e' quella di usare informazioni sulle tracce (on line reconstruction ~ 1 MHz) nel "trigger di primo livello" (LHCb, BTeV)



Resistenza alle radiazioni:

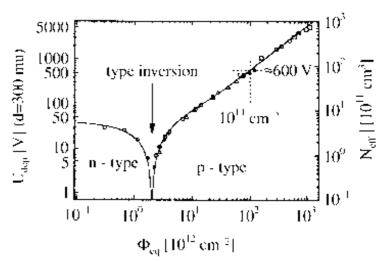
La "vita utile" di un rivelatore a Si e' funzione della quantita' di energia depositata dalle particelle sotto forma di "non-ionising energy loss" nel corpo del rivelatore:

- → Genera un cambiamento nella concentrazione "efficace" di drogante nel materiale (un materiale di "tipo n" diviene un materiale di "tipo p") con un effetto sulla tensione di svuotamento del rivelatore
- → Genera un aumento della corrente di perdita con l'aumentare della fluenza
- → Genera una diminuzione nella vita media dei portatori con una conseguente perdita nel segnale elettrico

Il problema viene affrontato con "device engineering" → collaborazione RD50

Table 1 Expected fluences of diffferent particles for 10 years of full luminosity running at $L=10^{34}\,\rm cm^{-2}\,s^{-1}$

Radius	π	р	n	Total	
		[×10 ¹²	$[\times 10^{14} \text{ particle/cm}^2]$		
10 cm 30 cm	5 1	1 0.1	1.1 0.8	~ 8 ~ 2	





Elettronica di Front-end:

L'amplificazione dei segnali "relativamente piccoli" generati nei rivelatori a Si varia con il rivelatore

pixel con spessori ~ 200 μ m \rightarrow 16000 coppie e-h strip con spessori ~ 300 – 400 μ m \rightarrow 36000 coppie e-h

Ad alte luminosita' (LHC, upgrade del Tevatron) l'elettronica per Pixel e Strip deve soddisfare a requisiti stringenti:

- essere a basso rumore
- possedere la capacita' di trattenere tutte le informazioni provenienti dal rivelatore in attesa di un segnale di trigger
- l'elettronica deve essere resistente alle radiazioni tanto quanto il rivelatore (almeno per i pixel)
- → L'architettura dell'elettronica di front-end e' quindi influenzata soprattutto da due parametri:
 - → Level 1 trigger rate
 - → Occupancy



Elettronica di Front-end:

Tre possibili scenari per gli esperimenti a collider:

1. Bassa occupancy con trigger rate < 1KHz (es. B-factory e+/e-)

2. Alta occupancy con trigger rate ~ 100 KHz – 1 MHz (es. Collider Adronici)

3. Altissima molteplicita' ma basso trigger rate (es. Collider a ioni pesanti)

→ Nel primo e nel terzo caso:

- il tempo di formatura e' relativamente lungo
- Il canale di elettronica e' strutturato in modo "tradizionale"
- Le uscite dei canali vengono multiplexate e mandate all'elettronica di "Backend"

→ Nel secondo caso:

- La banda passante del canale di lettura deve essere molto alta (~ 25 ns shaping time, determinato in gran parte dall'occupanza)
- I dati devono essere conservati in "lunghe pipeline" prima di essere multiplexati e rilasciati all'elettronica di Back-end



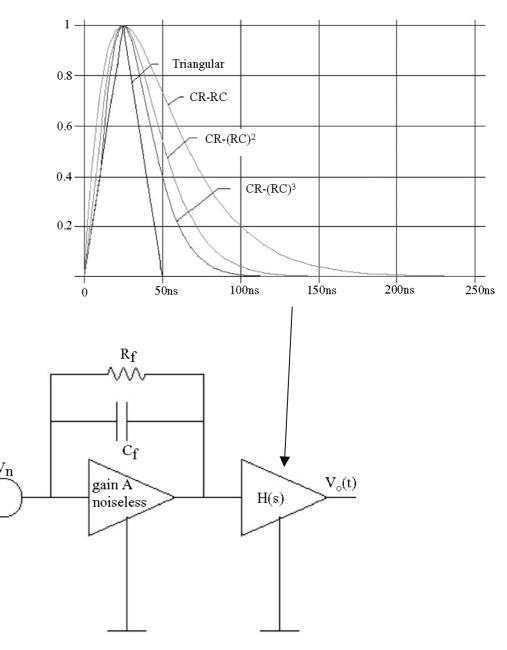
Front-end "tradizionale":

Rivelatore connesso ad un amplificatore di carica ideale seguito da un formatore con funzione di trasferimento H(s)

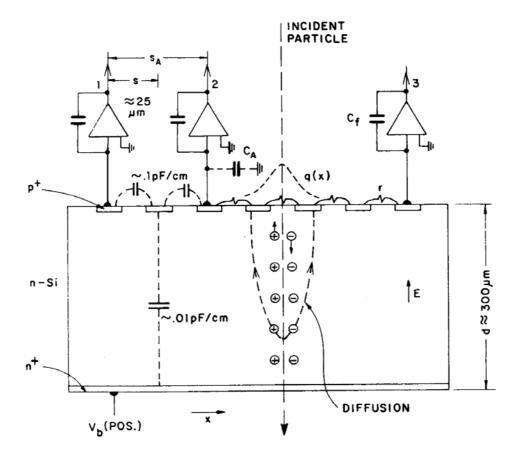
Si ottimizza il rapporto segnale/rumore come illustrato nelle precedenti lezioni

 $C_{\mathbf{d}}$

 $Q \delta(t)$







Rappresentazione schematica di un rivelatore a strip e della posizione della sua elettronica di lettura:

- la carica viene raccolta da piu' di un elettrodo → non tutte le strip debbono avere canali di lettura
- la posizione della traccia puo' essere ottenuta per divisione capacitiva (vedi canali 1 e 2) o resistiva (vedi canali 2 e 3)



Elettronica di Front-end per Babar

Un caso particolare dei precedenti e' l'esperimento BaBar (SLAC)

- il rivelatore di vertice e' costituito da cinque strati (~ 1 m^2) di rivelatore a strisce a doppia faccia
- tempo fra due "bunch crossing": ~ 4.2 ns
- trigger latency and jitter: 11.5 +/- 0.5 μsec
- maximum average trigger rate: 10 kHz
- maximum hit rate per channel: 150 kHz
- minimum input signal charge: 0.94 fC

.....

- time stamp accuracy: < 100 ns
- → Poiche' il bunch crossing e' molto frequente, nessuna delle operazioni di elaborazione del segnale debbono essere limitate a questo intervallo temporale
- → E' necessario che l'elettronica funzioni in modo asincrono, ovvero senza un clock per acquisire i segnali o per determinare quando analizzare il prossimo hit



Elettronica di Front-end per Babar

I requisiti della fisica si traducono nei parametri progettuali dell'elettronica:

- 0) Necessita' di una lettura analogica del segnale (minima risoluzione: 3 bit) per migliorare la risoluzione sull'impact parameter (attraverso divisione di carica fra le strisce)
- 1) Acquisizione e "processazione" del segnale in parallelo per tutti i canali
- 2) ENC: ~1200 el. rms
- 3) Sog lia del comparatore: 0.8 fC
- 4) Tempo di picco: per ragioni di rumore → 100 ns nei due layer piu' interni, piu' lungo sui layer piu' esterni (200ns, 300 ns e 400 ns)
- 5) Buffering degli eventi (a vari livelli), in modo che solo gli eventi sopra la soglia vengano trasmessi ("sparse readout") e che si possa usare un'alta frequenza di trasmissione (60 Mb/s).
- 6) Potenza dissipata per canale: < 4 mW
- **→** Metodo adottato per la lettura analogica del segnale **→** Time-over-Threshold (TOT)

Carica del rivelatore Q → picco del segnale all'uscita del formatore → tempo sopra la soglia di un comparatore (viene introdotta una compressione!!)

Mauro Citterio - 28 Ottobre 2004

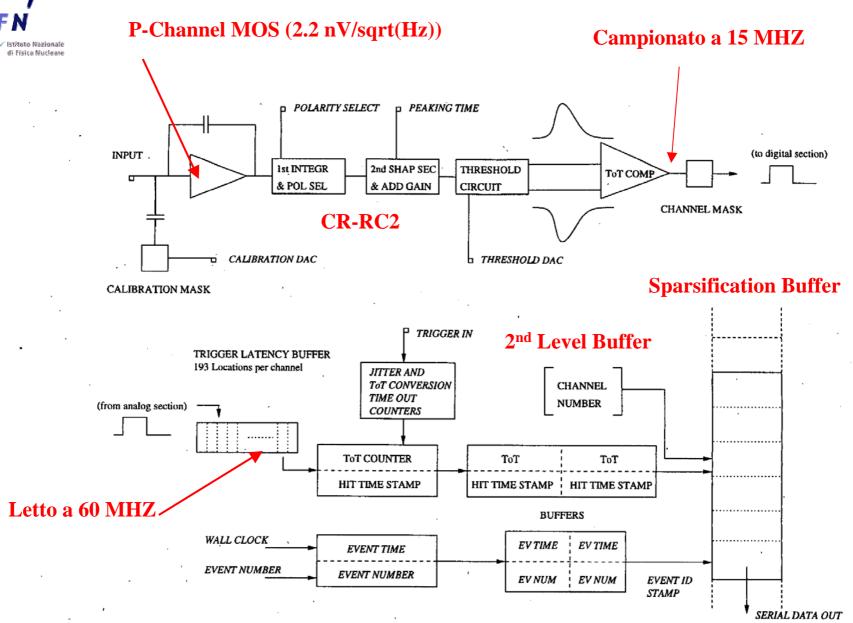


Figure 1: Architecture of the AToM chip. For each chip there are 128 identical channels.



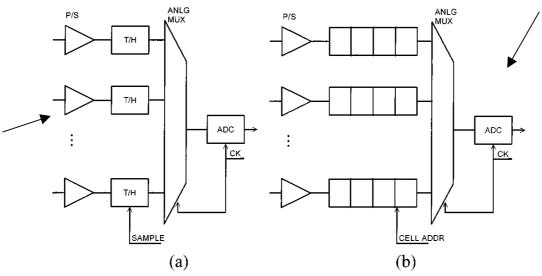
Metodologie generali di processamento dei dati

- Digitalizzazione immediata del segnale all'uscita del PA (e del filtro antialiasing). Tutte le operazioni di filtraggio, rilevamento del picco, etc ... nel dominio digitale.
- Concentrare i dati analogici prima di convertirli con un ADC
 - metodo del track and hold
 - metodo delle pipeline/memorie analogiche

- simili problemi

- necessita di un trigger preciso - ha un lungo dead time durante la conversione sequenziale - a bassa occupancy digitalizza spesso

"pedestals"



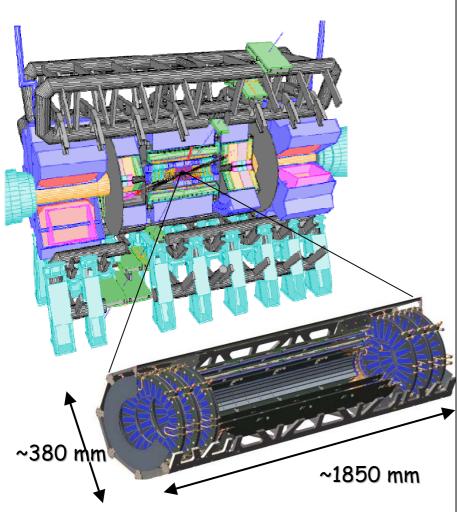
il tempo morto puo' essere minimizzato a patto di avere "extra" celle di buffer ed un controllore complesso

Fig. 1. Popular analog data concentration techniques. (a) The track-and-hold.

(b) The switched-capacitor analog memory.



Il rivelatore a Pixel di Atlas



- Il Pixel Detector e' il rivelatore di vertice dell'esperimento.
- Composto da tre layer nella regione del Barrel (B-layer a R=5.1 cm dalla regione di intersezione) e sei dischi, fornisce tre precisi punti di misura per la regione fino a $|\eta| < 2.5$.
- Composto da 1456 moduli per il barrel e 288 moduli per le regioni "forward"
- 80 milioni di canali di lettura con un area sensibile di 1.7 m².
- Moduli operano alla temperatura inferiore allo 0°C ed all'interno di un campo magnetico solenoidale di 2T.
- I moduli del barrel hanno un'inclinazione di 20° nel piano Rφ per "correggere" l'angolo di

Lorentz.

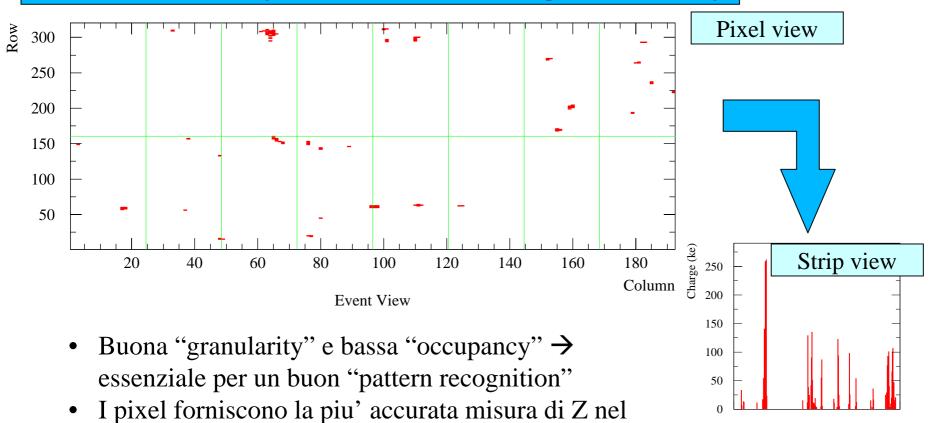


Perche' usare pixel in prossimita' del fascio?

Perche' altrimenti la ricostruzione degli eventi sarebbe molto
piu' complessa

Event in the B-layer (R=51 mm) at high luminosity

sistema di tracciamento di ATLAS.

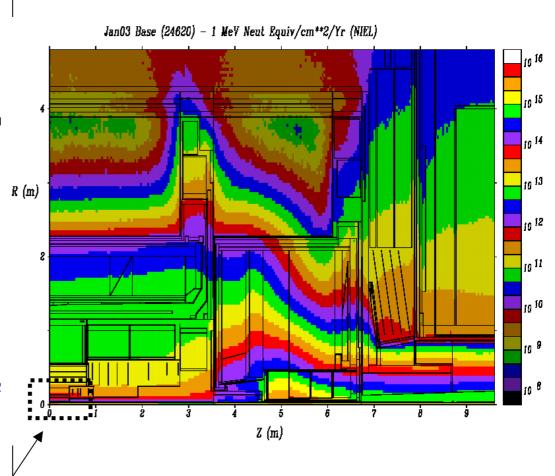




Simulazione della radiazione di fondo nell'apparato sperimentale

- Lo strato piu' esterno (R=8.8 e 12.1 cm) riceve una dose annuale di NIEL corrispondente alla fluenza di 10¹⁴ n_{eq}/cm²
- B-layer a R=5.1 cm riceve tre volte piu' radiazione dello strato esterno.
- Il rivelatore deve resistere alla dose ricevuta dallo strato piu' esterno durante dieci anni di operazione, ovvero:
 - NIEL > $10^{15} n_{eq}/cm^2$
 - dose >50 MRad

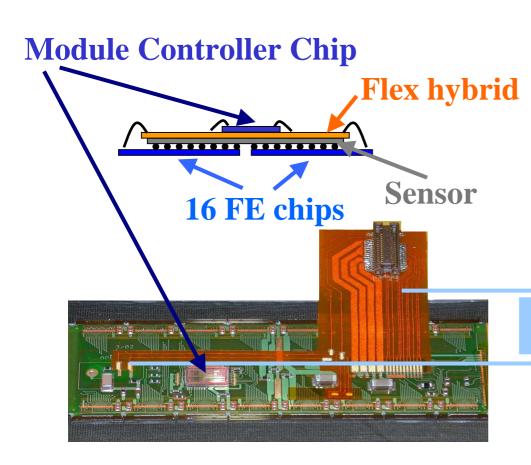
Tutti i componenti del rivelatore sono stati testati per questa condizione operativa (attraverso irraggiamenti accelerati)



Rivelatore a Pixel



Il concetto di modulo



- A module is the elementary self consistent detector unit.
- It consists of a **silicon sensor** read-out by 16 **front-end** (**FE**) **chips** connected **via bump bonding** (either SnPb at IZM, Berlin, or In at AMS, Rome).
- Data digitization is performed locally by the FE.
- Information from and to the FEs passes through a Module Controlle Chip, which also performs the event building.
- All communications use low voltage differential signal on micro-cables before being converted in optical signals at the end of the whole pixel detector active area.

Pigtail

HV connection



Pixeldetector Module

Module Controller Chip

Ogni modulo:

- contiene 46080 canali
- ha un'area attiva di 10 cm²

Second data link is required

Optical

Package

TTC

only for B-layer modules, due to higher occupancy

VCSEL2-

VCSEL

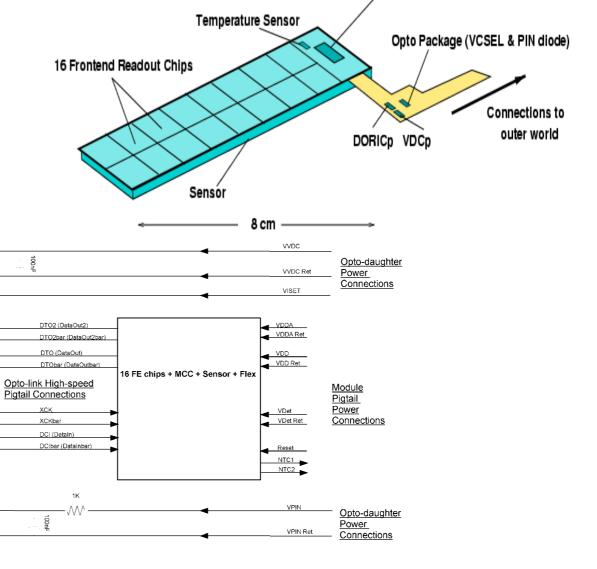
VDC-p Chip

DORIC-p Chip

VVDC Ret

VVDC

- dissipa: ~ 5W





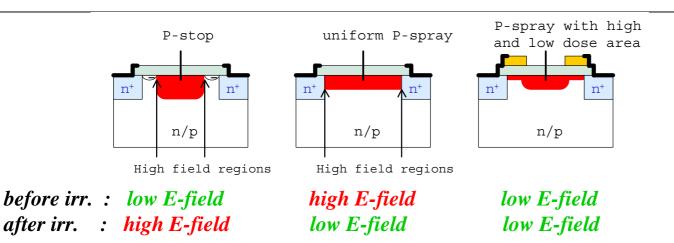
Il concetto di "Sector" e di "Stave"





Module's bricks: rad-hard sensors

- Sensor modules consists of 47232 n^+ pixels (mostly 50 μ m × 400 μ m) on n substrate, having an active area of 60.8×16.2 mm².
- Pixels are insulated by a moderated p-spray implant.
- For sensor testing all pixel can be kept equipotential by a bias grid.
- One full module is read out by 16 FE chips. Hybridization tolerences require at least 200 µm between adjacent chips. In order not to loose coverage, special pixel layout is chosen in these regions (long and ganged pixels).
- Test devices of single FE-chip size are also built for characterization.





Profondita della regione di svuotamento per "strutture" irraggiate

The ATLAS Pixel collaboration has been studying since 1998 silicon detectors irradiated up to the design value.

Oxygenated silicon detectors
irradiated up to a fluence of

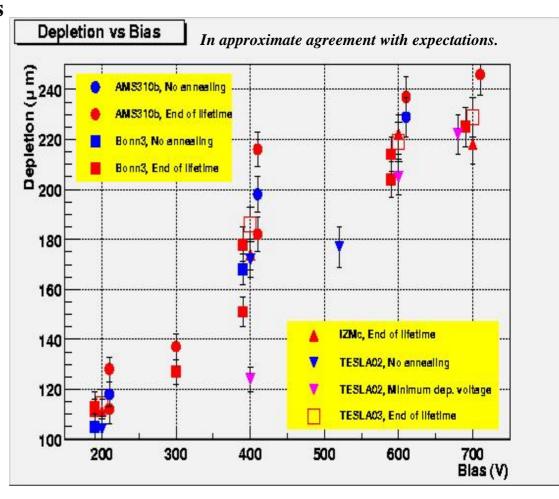
1.1×10¹⁵ cm⁻² 1 MeV neutron
equivalent are fully depleted at 600

V (planned maximum operation voltage).

The charge collection efficiency is

- 72±14 % if no annealing is performed on the sensor
- 87±14 % if a controlled annealing is performed during the LHC shutdown periods (about 2 weeks at room temperature)

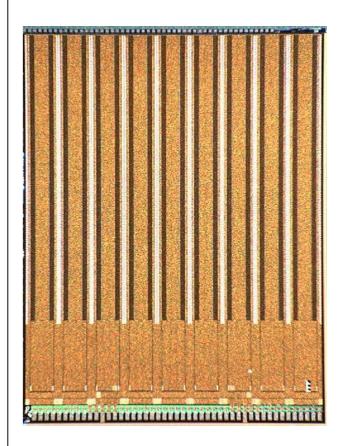
Lifetime of charge carriers is in the 4 ns range.





Module's brick: rad-hard FE Electronics

- The front-electronics chip, FE-I, is built in 0.25 μm IBM technology:
 - First version, I1, tested in 2002.
 - Improved version, I2, has been available since beginning of 2003. Production version I3 has been delivered in December 2003.
 - Each chip reads out 2880 pixels, arranged in column pairs.
 - Each pixel cell consists of a fast preamplifier followed by a discriminator
- It performs a sparse readout and store hits in EndOfColumn buffers, until the level 1 trigger latency is expired.
- **Threshold** can be adjusted by a 7-bit tuning DAC in each channel.
- **8-bit pulse height information** is obtained by the **Time-over-Threshold** technique. ToT uniformity is obtained by a 3-bit tuning DAC





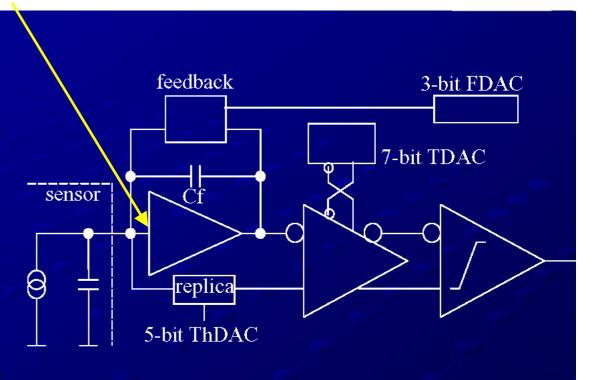
Pixel FE chip requirements:

- Threshold of about 4Ke for full efficiency and threshold dispersion less than about 200e (after tuning).
- Available threshold range:1-6Ke
- Total ENC less than about 300e after irradiation
- Radiation tolerance to 60Mrad
- leakage current tolerance of up to 100nA
- timewalk (time slewing from large charge to small charge) of less than 20ns for "intime" threshold of 4Ke. For example, operate with a threshold of 3Ke and an overdrive for 20ns slewing of 1Ke.
- Operate with nominal capacitive load of 400fF, about 25% parasitic to ground, and 75% to neighbors
- Should recover from 1 million electrons within ~microseconds.
- Modest charge measurement resolution of 4-5 bits
- Cross-talk less than 5-10% (pulse height in neighbor channel of 10-20 times threshold required to fire pixel)



PMOS input device

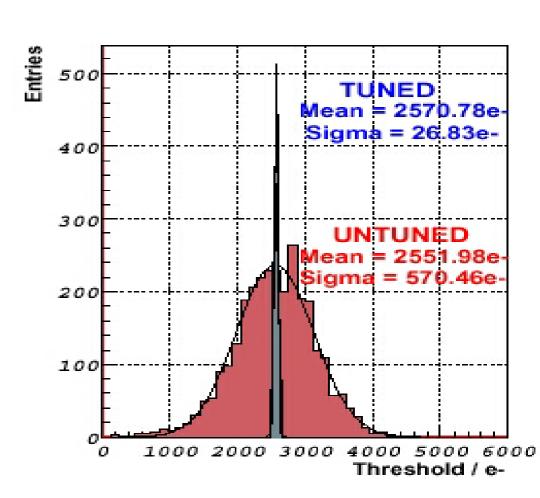
- Single power supply (1.6V)
- Power consumption: 30μW
- 2-stage based front-end (DC coupled)
- The preamp is single-ended and uses a replica voltage circuitry to drive the fully differential second stage
- Differential threshold setting
- The feedback capacitance is 5/6fF
- The preamp DC feedback performs a constant current discharge of the feedback capacitance and also deals with the sensor leakage current
- Features a kill mechanism which allows for switching off noisy or untunable pixels without changing their power consumption (no voltage drop during tuning)





FE-I characteristics: Threshold

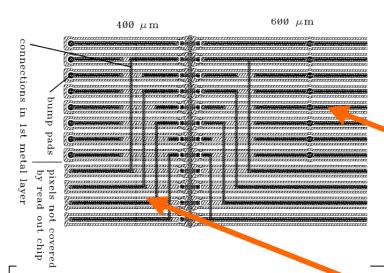
- The unadjusted threshold of the discriminators has a width of 600-900 e.
- Threshold can be adjusted by a 7-bit tuning DAC in each channel.
- After adjusting threshold dispersion in 25-40 e before irradiation.
- It has been measured to be about 80 e after 100 MRad dose.
- With no tails!
- Test beam data with I2 module were taken without masked channel and **NO random noise** has been observed.



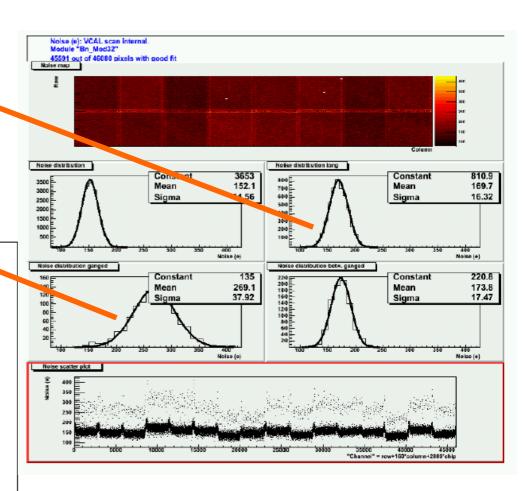
La correzione di soglia e' quasi piu' importante del rumore!



FE-I characteristics: Noise



- Noise is approximately:
 - 150 e for standard pixels
 - 170 e for long pixels (in the inter-chip region)
 - 270 e for ganged pixels (in the inter-chip region)
- It is of the order of 250 e after irradiation, the increase is due to the additional leakage current.





AMS - In



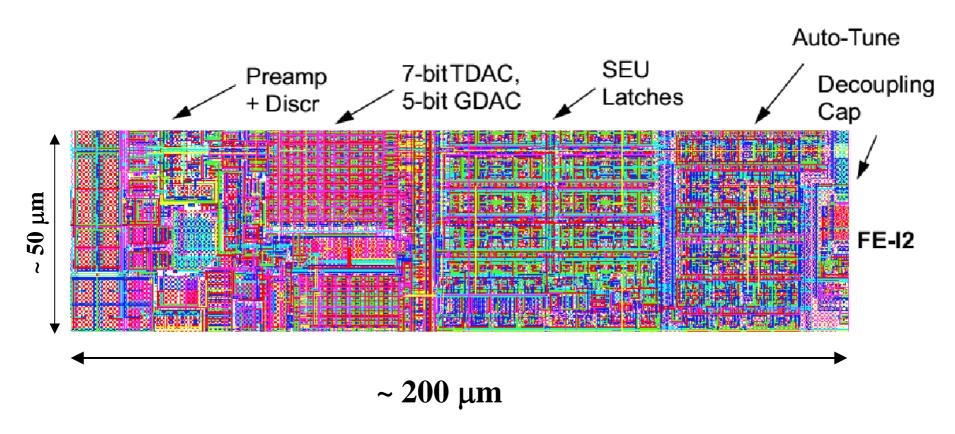
Bump bonding

- FE electronics is connected to the sensor cells using bump bonds.
- Two techniques, from different manufacturers will be used for production modules:
 - In bumps by Alenia-Marconi Systems, Rome
 - PbSn bumps by Fraunhofer-Institut für
 Zuverlässigkeit und Mikrointegration, Berlin
- Bumping defects can be investigated by X-ray inspections, or electrical tests, and now are very rare: the production contract fixes a rejection ratio of 150 faulty bumps/modules (0.3%).





Layout of one channel of the Front end electronics

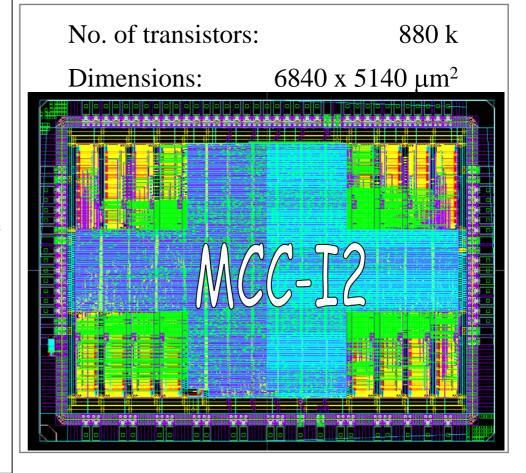


Il chip contiene ~ 2.5 M di transistori



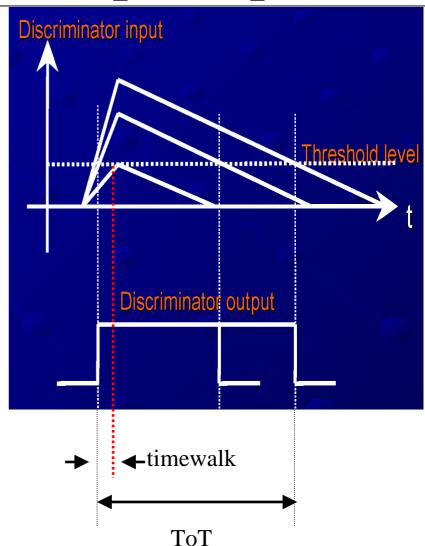
Module's brick: the MCC

- The Module Controller Chip is built in the same technology as the FE.
- Between the I1 and the I2 version some updates were included to improve SEU resistance:
 - all critical registers are tripled and use a majority decision logic;
 - in the FIFO's, where data are stored, a bit-flip safe encoding is used to unambiguously disentangle hits (for which a small corruption rate is acceptable) from event separators (whose loss would cause DAQ misalignment)
- At the PS irradiation facilities
 MCC were run for the equivalent
 100000 s at the B-layer, without
 the need to reconfigure the chip.



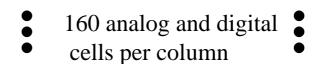


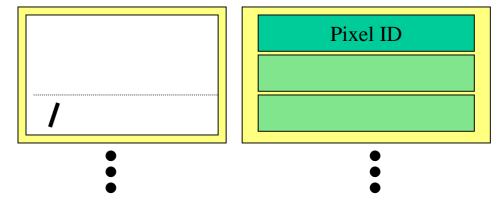
- 1) Beam interaction, particles cross the detector.
- 2) The preamplifier exceeds threshold: BCO id is memorized in the pixel cell, since this time depends on pulse height there is a timewalk effect.
- 3) the current feedback brings back the preamplifier signal below threshold: the trailing edge BCO id is stored in the pixel cell: this define the Time over Threshold in units of the 40 MHz clock cycle.
- 4) The pixel communicates it is ready for readout and within few clock cycles the hit data are stored in end of column buffers.
- 5) After trigger latency is elapsed the hit is either serialized for readout or deleted.



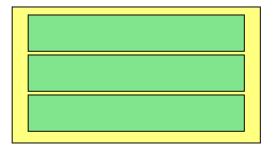


1) Beam interaction, particles cross the detector





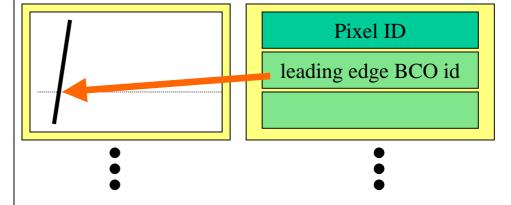
End of Column logic

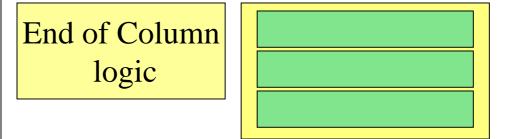




- 1) Beam interaction, particles cross the detector
- 2) The preamplifier exceeds threshold: BCO id is memorized in the pixel cell

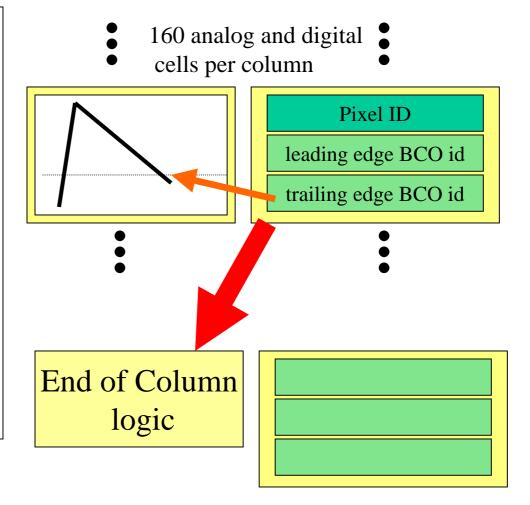
160 analog and digital cells per column





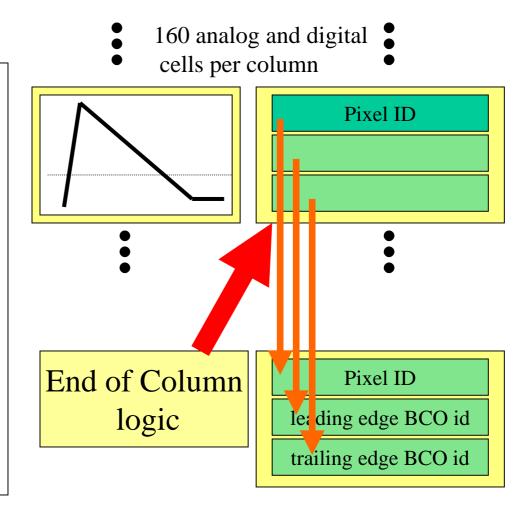


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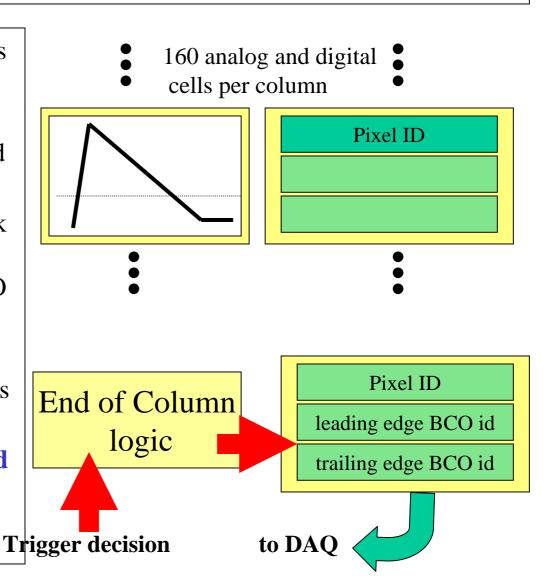


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- 4) within few clock cycles the hit is stored in end of column buffer.





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Conclusioni:

L'elettronica di front-end deve:

- poter operare a tempi di formatura dell'ordine delle decine di ns
- essere resistente alle radiazioni
- consumare poca potenza visto l'altissimo numero di canali
- essere in grado di svolgere sia funzioni analogiche che digitali
- → La grande maggioranza degli esperimenti si sta orientando verso l'uso di tecnologia CMOS a canale submicrometrico (IBM, TSMC) soprattuto quando sono necessari molti canali di lettura
- → Accurati modelli analogici dei dispositivi non sono sempre disponibili
- → I circuiti integrati arrivano ad avere oltre il milione di transistori e richiedono pool di progettisti
- → I software di progettazione e di verifica sono complessi e "time demanding"
- → La buona riuscita di un front-end dipende fortemente dal suo layout (per minimizzare effetti parassiti o indesiderati)





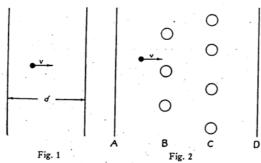
Currents Induced by Electron Motion*

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Summary—A method is given for computing the instantaneous current induced in neighboring conductors by a given specified motion of electrons. The method is based on the repeated use of a simple equation giving the current due to a single electron's movement and is believed to be simpler than methods previously described.

Introduction

N designing vacuum tubes in which electron transit-time is relatively long, it becomes necessary to discard the low-frequency concept that the instantaneous current taken by any electrode is proportional to the number of electrons received by



it per second. Negative grids, it is known, may carry current even though they collect no electrons and current may be noted in the circuit of a collector during the time the electron is still approaching the collector. A proper concept of current to an electrode must consider the instantaneous change of electrostatic flux lines which end on the electrode and the methods given in the literature for computing induced current due to electron flow are based on this concept.

A method of computing the induced current for a specified electron motion is here explained which is believed to be more direct and simpler than methods previously described. In the more difficult cases, in which flux plots or other tedious field-determination methods must be used, only one field plot is needed by the present method while the usual methods require a large number.

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METHOD OF COMPUTATION

The method is based on the following equation, whose derivation is given later:

$$i = E_r e v \tag{1}$$

where i is the instantaneous current received by the given electrode due to a single electron's motion, e is the charge on the electron, v is its instantaneous velocity, and E_v is the component in the direction v of that electric field which would exist at the electron's instantaneous position under the following circumstances: electron removed, given electrode raised to unit potential, all other conductors grounded. The equation involves the usual assumptions that induced currents due to magnetic effects are negligible and that the electrostatic field propagates instantaneously.

SIMPLE EXAMPLE

A simple example is offered in the computation of the instantaneous current due to an electron's motion between two infinite plates (Fig. 1). (The result is a starting point for the analysis of a diode, for example, when the transit-time is long.)

From (1) we obtain immediately

$$i = evE_v = \frac{ev}{d}$$

In the literature it is stated that this same result is deduced from image theory. This involves the setting up of an infinite series of image charges on each side of the plates for a given position of the electron and a consideration of the total flux crossing one of the planes due to the series of charges, a method which is lengthy and requires no little familiarity with methods of handling infinite series.

THE GENERAL CASE

Consider a number of electrodes, A, B, C, D, in the presence of a moving electron (Fig. 2) whose path and instantaneous velocity are known. A tedious way to find the current induced in, say, electrode

¹ D. O. North, "Analysis of the effects of space charge on grid impedance," Proc. I.R.E., vol. 24, pp. 108-158; February, (1936).



A is to make a flux plot of the lines of force emanating from the electron, when it is at some point of its path, and note the portion of the total lines which end on A. By making a number of such plots it is possible to observe the change in the number of lines ending on A as the electron moves, and consequently to compute the induced current. The accuracy is dependent upon the number of plots made.

It is much simpler to use (1). One plot is made for the case of A at unit potential, B, C, D grounded, and the electron removed, E_v is then known and

$$i = E_v ev.$$

To minimize the induced current in a negative grid, an important consideration in the design of high-frequency amplifiers and oscillators, it may be that (1) will prove helpful to the designer. The equation states that the electrode configuration should be such as to yield minimum E_{\bullet} . If the electron's path, for example, is made to coincide with an equipocential of the grid (not an equipotential in the field in which the electron is traveling, of course, but an equipotential in that artificial field due to unit potential on the grid, the electron removed, and all else grounded) the induced current will be zero. It will not be possible to realize this for the complete electronic path, since the electron must start at some equipotential surface, but it may be possible to find practical configurations that will approach this condition over a good share of the path.

DERIVATION OF EQUATION (1)

Consider the electron, of charge e, in the presence of any number of grounded conductors, for one of which, say A, the induced current is desired. Surround the electron with a tiny equipotential sphere. Then if V is the potential of the electrostatic field, in the region between conductors

$$\nabla^2 V = 0$$

where ∇^2 is the Laplacian operator. Call V_{\bullet} the potential of the tiny sphere and note that V=0 on the conductors and

$$-\int \frac{\partial V}{\partial n} ds = 4\pi e \qquad \text{(Gauss' law)}$$
sphere's surface

where $\partial V/\partial n$ indicates differentiation with respect to the outward normal to the surface and the integral is taken over the surface of the sphere.

Now consider the same set of conductors with the electron removed, conductor A raised to unit potential, and the other conductors grounded. Call the potential of the field in this case V', so that $\nabla^2 V' = 0$ in the space between conductors, including the point

where the electron was situated before. Call the new potential of this point V_{\bullet}' .

Now Green's theorem² states that

$$\int_{\text{volume}} [V'\nabla^2 V - V\nabla^2 V'] dv$$
between
boundaries
$$= -\int_{\text{boundary}} \left[V'\frac{\partial V}{\partial n} - V\frac{\partial V'}{\partial n}\right] ds. \qquad (2)$$
surfaces

Choose the volume to be that bounded by the conductors and the tiny sphere. Then the left-hand side is zero and the right-hand side may be divided into three integrals:

- Over the surfaces of all conductors except A.
 This integral is zero since V = V' = 0 on these surfaces.
- (2) Over the surface of A. This reduces to $-\int (\partial V)/(\partial n)ds$, surface A

for V'=1 and V=0 for conductor A.

(3) Over the surface of the sphere. This becomes

$$-V.\int \frac{\partial V}{\partial n} ds + V.\int \frac{\partial V'}{\partial n} ds.$$
sphere's surface sphere's surface

The second of these integrals is zero by Gauss' law since $\int (\partial V')/(\partial n)ds$ is the negative of the charge enclosed (which was zero for the second case in which the electron was removed).

Finally, we obtain from (2)

$$0 = -\int \frac{\partial V}{\partial n} ds - V \cdot' \int \frac{\partial V}{\partial n} ds$$
surface A sphere's surface
$$= 4\pi Q_A + 4\pi eV \cdot'$$

$$Q_{A} = -eV.'$$

$$i_{A} = \frac{dQ_{A}}{dt} = -e \frac{dV.'}{dt} = -e \left[\frac{\partial V.'}{\partial x} \frac{dx}{dt} \right]$$

where x is the direction of motion.

Now

$$\frac{dx}{dt} = v \quad \text{and} \quad \frac{\partial V_{\star}'}{\partial x} = -E_{\star},$$

$$i = \epsilon v E_{\star}. \tag{1}$$

J. H. Jeans, "Electricity and Magnetism," page 160, Cambridge, London, England, (1927).